DISPLAY DEVICE

Patent number: JP4166891 (A) Publication date: 1992-06-12

Inventor(s): ISHIZUKA KUNIMITSU

Applicant(s): FUJITSULTD

Classification:
- international: H04N5/04: G09G5/12: G09G5/18: H04N5/04: G09G5/12: G09G5/18:

#ternational: H04N5/04; G09G5/12; G09G5/18; H04N5/0 (IPC1-7): G09G5/12; G09G5/18; H04N5/04

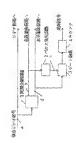
- european:

Application number: JP19900293088 19901030

Priority number(s): JP19900293088 19901030

Abstract of JP 4166891 (A)

PURPOSE: To identify a display mode without adding a signal line by providing a counting means for counting horizontal synchronizing pulses and equalizing pulses included in the pulse period of a single pulse, and identifying the display mode by means of the output of the counting means. CONSTITUTION: A vertical synchronizing pulse b separated by a synchronous separation circuit 1 triggers a pulse generating circuit 2 so as to generate a single pulse (c) having a specified pulse period. The single pulse (c) is inputted to a gate circuit 3 to open a gate only during the pulse period. On the other hand, a horizontal synchronizing pulse and an equalizing pulse (d) separated by the synchronous separation circuit 1 are passed through the gate circuit 3 to be sent to a counter 4. The counter 4 counts the pulse number of horizontal synchronizing pulses and equalizing pulses during this pulse period and outputs a signal which corresponds to the number of counts. Thus, a display mode can be identified without adding a signal line.



Data supplied from the esp@cenet database — Worldwide